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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,837	11/25/2002	Peter B. Gray	BUR920010190	9703

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,837	GRAY ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the request for continued examination filed June 8, 2004.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered **(See Specification Paragraph 4)**.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamaguchi et al. *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors*.

In regards to claim 6, Yamaguchi et al. ("Yamaguchi") discloses the following:

a) a single layer of silicon that forms an emitter region of the PNP transistor, an extrinsic base region of the NPN transistor and an intrinsic base region of the NPN transistor (For Example: See Figure 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5, 7 and 9 are rejected under 35 U.S.C. 103(a) as obvious over Yamaguchi et al. *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors* and Babcock et al. (U.S. Publication No. 2003/0080394).

In regards to claim 1, Yamaguchi discloses the following:

a) an emitter of the vertical PNP transistor (For Example: See Figure 1); and

b) an extrinsic base region of the vertical NPN transistor and an intrinsic base region of the vertical NPN transistor located in the same layer as the emitter region of the vertical PNP transistor (For Example: See Figure 1).

In regards to claim 1, Yamaguchi fails to disclose the following:

a) the emitter region of the PNP transistor includes silicon and germanium.

However, Babcock discloses the use of an emitter containing silicon and germanium (For Example: See Paragraph 34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include use of an emitter containing silicon and germanium as disclosed in Babcock because it aids in providing a device where balance is facilitated (For Example: See Abstract and Paragraphs 12-23).

Additionally, since Yamaguchi and Babcock are both from the same field of endeavor, the purpose disclosed by Babcock would have been recognized in the pertinent art of Yamaguchi.

In regards to claim 2, Yamaguchi fails to disclose the following:

a) the maximum germanium concentration makes up no less than 10% of the silicon and germanium, and wherein the maximum germanium concentration makes up no more than 30% of the silicon and germanium.

However, the applicant has not established the critical nature of "the maximum germanium concentration makes up no less than 10% of the silicon and germanium, and wherein the maximum germanium concentration makes up no more than 30% of the silicon and germanium." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 3, Yamaguchi fails to disclose the following:

a) the silicon is polysilicon.

However, Babcock discloses the use of polysilicon (For Example: See Paragraph 34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include use of polysilicon as disclosed in Babcock because it aids in providing a device where balance is facilitated (For Example: See Abstract and Paragraphs 12-23).

Additionally, since Yamaguchi and Babcock are both from the same field of endeavor, the purpose disclosed by Babcock would have been recognized in the pertinent art of Yamaguchi.

In regards to claim 5, Yamaguchi fails to disclose the following:

a) the emitter region also includes carbon.

However, Babcock discloses the use of carbon (For Example: See Paragraph 34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include the use of carbon as disclosed in Babcock because it aids in providing a device where balance is facilitated (For Example: See Abstract and Paragraphs 12-23).

Additionally, since Yamaguchi and Babcock are both from the same field of endeavor, the purpose disclosed by Babcock would have been recognized in the pertinent art of Yamaguchi.

In regards to claim 7, Yamaguchi fails to disclose the following:

a) the emitter region of the PNP transistor includes silicon and germanium.

However, Babcock discloses the use of an emitter containing silicon and germanium (For Example: See Paragraph 34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include use of an emitter containing silicon and germanium as disclosed in Babcock because it aids in providing a device where balance is facilitated (For Example: See Abstract and Paragraphs 12-23).

Additionally, since Yamaguchi and Babcock are both from the same field of endeavor, the purpose disclosed by Babcock would have been recognized in the pertinent art of Yamaguchi.

In regards to claim 9, Yamaguchi fails to disclose the following:

a) the emitter region also includes carbon.

However, Babcock discloses the use of an emitter containing carbon (For Example: See Paragraph 34). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include use of an

emitter containing carbon as disclosed in Babcock because it aids in providing a device where balance is facilitated (For Example: See Abstract and Paragraphs 12-23).

Additionally, since Yamaguchi and Babcock are both from the same field of endeavor, the purpose disclosed by Babcock would have been recognized in the pertinent art of Yamaguchi.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as obvious over Yamaguchi et al. *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors* in view of Babcock et al. (U.S. Publication No. 2003/0080394) and Goth (U.S. Patent No. 4,719,185).

In regards to claim 4, Babcock fails to disclose the following:

a) the transistor has a cutoff frequency greater than 1 GHz.

However, Goth discloses the use of a transistor with a cutoff frequency greater than 1 GHz (For Example: See Column 4 Lines 13 and 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Babcock to include use of a transistor with a cutoff frequency greater than 1 GHz as disclosed in Goth because it aids in providing a device with low power consumption characteristics (For Example: See Column 3 Lines 44-68 and Column 4 Lines 1-14).

Additionally, since Babcock and Goth are both from the same field of endeavor, the purpose disclosed by Goth would have been recognized in the pertinent art of Babcock.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as obvious over Yamaguchi et al. *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors*.

In regards to claim 8, Yamaguchi fails to disclose the following:

a) the maximum germanium concentration makes up no less than 10% of the silicon and germanium, and wherein the maximum germanium concentration makes up no more than 30% of the silicon and germanium.

However, the applicant has not established the critical nature of "the maximum germanium concentration makes up no less than 10% of the silicon and germanium, and wherein the maximum germanium concentration makes up no more than 30% of the silicon and germanium." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as obvious over Yamaguchi et al. *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors* in view of Babcock et al. (U.S. Publication No. 2003/0080394) and Harame et al. (U.S. Patent No. 4,997,776).

In regards to claim 10, Yamaguchi discloses the following:

a) the silicon layer is polysilicon in the emitter region of the PNP transistor, and silicon in a portion of the extrinsic base region and silicon in the intrinsic base region of the NPN transistor.

However, Harame discloses the use of a silicon layer that is polysilicon in the emitter region of the PNP transistor, and silicon in a portion of the extrinsic base region and silicon in the intrinsic base region of the NPN transistor (For Example: See Column 4 Lines 33-45, Column 6 Lines 31-58). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include the use of a silicon layer that is polysilicon in the emitter region of the PNP transistor, and silicon in a portion of the extrinsic base region and silicon in the intrinsic base region of the NPN transistor as disclosed in Harame because it aids in improving the performance of the device (For Example: See Column 1 Lines 64-68, Column 2 Lines 1-68 and Column 3 Lines 1-44).

Additionally, since Yamaguchi and Harame are both from the same field of endeavor, the purpose disclosed by Harame would have been recognized in the pertinent art of Yamaguchi.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as obvious over Yamaguchi et al. *Process and Device Optimization of an Analog Complementary Bipolar IC Technology With 5.5-GHz fT PNP Transistors* in view of Goth (U.S. Patent No. 4,719,185).

In regards to claim 11, Yamaguchi fails to disclose the following:

a) the transistor has a cutoff frequency greater than 1 GHz.

However, Goth discloses the use of a transistor with a cutoff frequency greater than 1 GHz (For Example: See Column 4 Lines 13 and 14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Yamaguchi to include use of a transistor with a cutoff frequency greater than 1 GHz as disclosed in Goth because it aids in providing a device with low power consumption characteristics (For Example: See Column 3 Lines 44-68 and Column 4 Lines 1-14).

Additionally, since Yamaguchi and Goth are both from the same field of endeavor, the purpose disclosed by Goth would have been recognized in the pertinent art of Yamaguchi.

Response to Arguments

11. Applicant's arguments filed 6/8/04 have been fully considered but they are not persuasive. Applicant has argued that Yamaguchi et al. ("Yamaguchi) does not teach a single layer that forms the emitter region of the PNP transistor and the extrinsic and intrinsic base regions of the NPN transistor. Claim 6 merely requires a single layer of Si form the emitter region of the PNP transistor and the extrinsic and intrinsic base regions of the NPN transistor. Note in section II of the Yamaguchi article that it is taught that an N-type epitaxial layer having a thickness of 1.4 um is formed on the substrate, that is the silicon portion shown in figure 1 located above the dotted line. Hence, as is clear from figure 1 of Yamaguchi, the emitter region of the PNP transistor and the extrinsic and intrinsic base regions of the NPN transistor are formed from "a single layer of Si," as required in claim 6 or "located in same region," as required by claim 1.

Applicant has further argued that Yamaguchi does not disclose "sharing implants" for the emitter region of the PNP transistor and the extrinsic and intrinsic base regions of the NPN transistor. However, the claim does not require these regions to be formed from a "shared implant." Applicant's arguments are clearly not commensurate in scope with the claims as presently written. As noted above, Yamaguchi clearly teaches the formation of an epitaxial layer in which the emitter of the PNP transistor and extrinsic and intrinsic base region of the NPN transistor are formed, however, these regions are formed in "a single layer of silicon" as required by the claims.

Finally, Applicant has argued that "there is no suggestion or motivation to combine Yamaguchi et al. and Babcock et al...SiGeC is used to retard the diffusion of the common P-type dopant...retarding diffusion of p-type dopant is not a concern in Yamaguchi et al." However, using SiGeC would retard diffusion and aid in keeping the emitter and base from spreading. Yamaguchi need not recognize this problem or any possible solution to the problem in order to be properly combined with Babcock et al.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
August 16, 2004

Mary Wilczewski
Primary Examiner